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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Inventor :	Christopher M. Giles	Group Art Unit: 2111
Appln. No.:	10/027,936	Examiner: X. M. Thai
Filed :	December 21, 2001	
For :	REUSABLE COMPLEX MULTI-BUS SYSTEM HARDWARE PROTOTYPE SYSTEM	
Docket No.:	01-297/L13.12-0180	

RESPONSE

Commissioner for Patents
P.O. Box 1450
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I HEREBY CERTIFY THAT THIS PAPER IS BEING SENT BY U.S. MAIL, FIRST CLASS, TO THE COMMISSIONER FOR PATENTS, P.O. BOX 1450, ALEXANDRIA, VA 22313-1450, THIS
30th DAY OF September, 2004
PATENT ATTORNEY

Sir:

This is in response to the Office Action dated on June 30, 2004 in which claims 1-6, 8-9, 11-14, 16 and 17 were rejected, and claims 7, 10 and 15 were objected to. With this Response, claims 1-17 remain unamended and are presented for reconsideration and allowance in view of the following discussion. Favorable action is respectfully requested.

In section 3 of the Office Action, claims 1-6, 13, 14, 16 and 17 were rejected under 35 U.S.C. §102(b) as being anticipated by Balakrishnan (U.S. Patent No. 5,122,691). In support of the rejection of claims 1, 13 and 17, the Office Action states that "Balakrishnan teaches a platform comprising: a backplane (Fig. 5) providing a plurality of busses; a plurality of system bus cards (90-107), each of the system bus cards comprising: a system bus (e.g. 83, fig. 6; col. 9, lines 49 et seq.; 171; fig. 7; col. 10, lines 3-10); a bus infrastructure device (e.g. bus chip(s); col. 9, lines 2-15); [and] a plurality of daughter cards (modules 110-117; col. 9, lines 1-35)." This interpretation of the Balakrishnan is respectfully traversed, as is the rejection of these pending claims.

Claim 1 is directed to a configurable and scalable multi-bus platform for developing, testing, and/or debugging prototype systems to be implemented in an integrated circuit. In

contrast, Balakrishnan teach a physical layer architecture for use in a computer system. Consistent with the fact that an architecture for use in a computer system is considerably different than a configurable and scalable multi-bus platform for developing, testing and/or debugging prototype systems to be implemented in an integrated circuit, the combination of claim limitations recited in independent claim 1 is not taught or suggested by Balakrishnan.

As recited in claim 1, the platform includes "a backplane providing a plurality of busses," and "a plurality of system bus card each physically coupleable to the backplane." As is further recited in independent claim 1, each of the plurality of system bus cards includes "a system bus which is electrically coupled to a corresponding one of the plurality of busses provided by the backplane when the system bus card is physically coupled to the backplane." Also as recited in claim 1, the platform further includes "a plurality of daughter cards each physically coupleable to one of the plurality of system bus cards and including at least one master or slave device." When a particular daughter card is physically coupled to one of the plurality of system bus cards, then "at least one master or slave device of the particular daughter card is in electrical communication with the system bus of the system bus card."

As mentioned above, in support of the rejection of independent claim 1, the Office Action asserts that Balakrishnan teaches a platform comprises a backplane providing a plurality of busses and a plurality of system bus cards, citing cards 90-107 as the system bus cards. However, this is in contrast to the teachings of Balakrishnan. To meet the claim limitations recited in independent claim 1, Balakrishnan must teach a backplane providing a plurality of busses, and a plurality of system bus cards each physically coupleable to the backplane. The system bus on each of the system bus cards must be electrically coupled to a corresponding one of the plurality of busses provided by the backplane when the system bus card is physically coupled to the backplane. The Office Action states that the backplane is shown in FIG. 5, and that the plurality of system bus cards are shown at elements 90-107 in that figure. However, the teachings of Balakrishnan make it clear that cards 90-107 are in fact the backplane, and not the system bus cards which are coupleable to the backplane. See for example Balakrishnan at col. 8, lines 63-65 which state that "FIG. 5 shows an implementation of the present invention wherein a bus

backplane consists of a plurality of cards 90-107." (emphasis added) Therefore, even if cards 90-107 of Balakrishnan are considered to be a backplane as recited in independent claim 1, Balakrishnan lacks a teaching or suggestion of a plurality of system bus cards each physically coupleable to the backplane, with each of the system bus cards including a system bus which is electrically coupled to a corresponding one of the plurality of busses provided by the backplane when the system bus card is physically coupled to the backplane. The fact that cards 90-107 together provide a backplane, as opposed to each being a system bus card as recited, is further illustrated at col. 9, lines 3-9 which state that for each of these cards an integrated circuit, also called a bus chip, may include a bit line of the bus along with the bus drivers and bus receivers for the bit line.

As noted above, the Office Action indicates that modules 110-117 taught by Balakrishnan meet the requirements of the plurality of daughter cards recited in independent claim 1. However, Balakrishnan makes it clear that these plug-in modules are not each coupleable to one of a plurality of system bus cards, with the system bus cards themselves coupleable to a backplane as is recited in the claim. Instead, in Balakrishnan, plug in modules 110-117 are coupled to the backplane provided by cards 90-107. Therefore, Balakrishnan further fails to meet this additional limitation of independent claim 1. In view of the fact that Balakrishnan fails to teach or suggest these elements as recited in independent claim 1, it is respectfully submitted that independent claim 1 and dependent claims 2-12 are in condition for allowance. Dependent claims 2-12 also contain further limitations which distinguish from the teachings of the cited art. Reconsideration and allowance of claims 1-12 are respectfully requested.

As mentioned above, independent claim 13 was rejected under the same grounds as independent claim 1. The basis of the rejection cited in the Office Action was as described above. Once again, the interpretation of Balakrishnan, and its application in rejecting independent claim 13, are respectfully traversed. Like independent claim 1, independent claim 13 is directed to a configurable and scalable multi-bus platform for developing, testing and/or debugging prototype systems to be implemented in an integrated chip. Also like independent claim 1, the platform recited in independent claim 13 includes a backplane providing a plurality of busses. The

platform also includes a plurality of substantially identical system bus cards each physically couplable to the backplane, which each of the system bus cards including a system bus which is electrically coupled to at least one of the plurality of busses provided by the backplane when the system bus card is physically coupled to the backplane. As recited, the platform also includes a plurality of daughter cards each physically coupleable to one of the plurality of system bus cards and including at least one master or slave device. As was described in detail with reference to the rejection of independent claim 1, it is respectfully submitted that Balakrishnan fails to teach or suggest this combination of limitations recited in independent claim 13.

As a specific example, it was demonstrated above that Balakrishnan does not teach a backplane and a plurality of system bus cards (cards 90-107 as cited in the Office Action), but instead teaches a backplane consisting of plurality of cards 90-107. Further still, Balakrishnan neither teaches nor suggests a plurality of daughter cards each physically coupleable to one of the plurality of system bus cards and including at least one master or slave device such that when a particular daughter card is physically coupled to one of the plurality of system bus cards, then at least one master or slave device of the particular daughter card is in electrical communication with the system bus of the system bus card. Lacking a teaching or suggestion of this combination of claim limitations, it is respectfully submitted that independent claim 13 and dependent claims 14-16 are in condition for allowance. Dependent claims 14-16 also contain additional limitations which distinguish from the cited art. Therefore, reconsideration and allowance of claim 13-16 are respectfully requested.

In the Office Action, independent claim 17 was also rejected as being anticipated by Balakrishnan, with the cited basis being as described above. Independent claim 17 includes claim limitations which are similar to those described above with reference to independent claims 1 and 13, which are neither taught nor suggested by Balakrishnan. Therefore, the rejection of independent claim 17 is respectfully traversed as well.

Specifically, independent claim 17 is directed to a configurable scalable and multi-bus platform for developing, testing, and/or debugging prototype systems to be implemented in an integrated chip. As recited, the platform includes "backplane means for providing a plurality of

busses." See for example backplane 305 illustrated in FIGS. 3 and 4. The recited platform also includes "bus card means coupled to the backplane means for providing a plurality of system busses coupled to the plurality of busses provided by the backplane means." See for example system bus cards 310 illustrated in FIGS. 3 and 4. Finally, the platform recited in independent claim 17 includes "daughter card means for configuring the bus card means in order to model a corresponding system bus on an integrated circuit to be implemented." See for example daughter cards 315 shown in FIGS. 3 and 5.

As it has been demonstrated above, Balakrishnan fails to teach or suggest a backplane means for providing a plurality of busses, in conjunction with bus card means which can be coupled to the backplane means for providing a plurality of system busses coupled to the plurality of busses provided by the backplane means. Further, Balakrishnan fails to teach or suggest daughter card means as recited. Further still, the daughter card means recited in independent claim 17 configure the bus card means in order to model a corresponding system bus on an integrated circuit to be implemented. Since Balakrishnan teach a physical layer architecture for use in a computer system, and not a multi-bus platform for developing, testing and/or debugging prototype system to be implemented in an integrated chip, it is clear Balakrishnan do not teach or suggest the limitation of the daughter card means configuring the bus cards means in order to model a corresponding system bus on an integrated circuit to be implemented. Lacking a teaching or suggestion of these cited claim limitations, it is respectfully submitted that independent claim 17 is also in condition for allowance.

In sections 5-7 of the Office Action, claims 8, 9, 11 and 12 were rejected under 35 U.S.C. §103 as being unpatentable over Balakrishnan in view of various prior art references. However, as demonstrated above, each of these claims is allowable based at least upon their dependence from patentable independent claims. The cited combinations of references fail to make up for the short comings of the teachings of Balakrishnan. Consequently, it is believed that all pending claims are in condition for allowance. Reconsideration and allowance of claims 1-17 are therefore respectfully requested.

The Director is authorized to charge any fee deficiency required by this paper or credit any overpayment to Deposit Account No. 23-1123.

Respectfully submitted,

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